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Q. 3.7: Simplify the following Boolean expressions, using four variable maps
(a) $w'z + xz + x'y + wx'z$

Q. 3.7: Simplify the following Boolean expressions, using four variable maps
(a) $w'z + xz + x'y + wx'z$
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Q. 3.7: Simplify the following Boolean expressions, using , four , -variable maps: (a) $w'z + xz + x'y + wx'z$ (b) $AD' + B'C'D + BCD' + \dots$

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Q. 3.5: Simplify the following Boolean functions, using four-variable maps: (a) $F(w,x,y,z) = \text{sum}(1,$

*Q. 3.5: Simplify the following Boolean functions, using four-variable maps: (a) $F(w,x,y,z) = \text{sum}(1,$
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following Boolean functions, using , four , -variable
maps: (a) $F(w,x,y,z) = \text{sum}(1,, 4 , ,5,6,12,14,15)$
(b) $F(A,B,C,D) \dots$*

Q. 4.1: Consider the combinational circuit shown

in Fig. P4.1.(a) Derive the Boolean expressions fo*

*Q. 4.1: Consider the combinational circuit shown
in Fig. P4.1.(a)* Derive the Boolean expressions fo*

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*Consider the combinational circuit shown in Fig.
P4.1. (a)* Derive the Boolean expressions for T1
through T4. Evaluate the ...*

*Q. 3.23. Implement the following Boolean function
F, together with the don't-care conditions d*

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Q. 3.23. Implement the following Boolean function F , together with the don't-care conditions d von Dr. Dhiman Kakati vor 1 Jahr 6 Minuten, 46 Sekunden 3.635 Aufrufe Q. 3.23. Implement the following Boolean function F , together with the don't-care conditions d , using no more than two NOR gates: ...

Q. 7.19: Tabulate the PLA programming table for the four Boolean functions listed below.

Q. 7.19: Tabulate the PLA programming table for

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the four Boolean functions listed below. von Dr. Dhiman Kakati vor 5 Monaten 7 Minuten, 28 Sekunden 1.542 Aufrufe

Q. 7.19: Tabulate the PLA programming table for the , four , Boolean functions listed below. Minimize the numbers of product terms.

Q. 4.19: Construct a BCD adder-subtractor circuit. Use the BCD adder of Fig. 4.21 and the 9's complement

Q. 4.19: Construct a BCD adder-subtractor circuit.

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Use the BCD adder of Fig. 4.21 and the 9's complementer of problem 4.18.

Q. 4.19: Construct a BCD adder-subtractor circuit. Use the BCD adder of Fig. 4.21 and the 9's complementer of problem 4.18.

[*Q. 4.11: Using four half-adders \(HDL—see Problem 4.54\), \(a\) Design a full-subtractor circuit incrementer*](#)

Q. 4.11: Using four half-adders (HDL—see Problem 4.54), (a) Design a full-subtractor circuit incrementer

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von Dr. Dhiman Kakati vor 11 Monaten 6 Minuten, 44 Sekunden 5.433 Aufrufe Q. 4.11: Using , four , half-adders (HDL—see Problem 4.54), (a) , Design , a full-subtractor circuit incrementer. (A circuit that adds one ...

[*Q. 1.1: List the octal and hexadecimal numbers from 16 to 32. Using A and B for the last two digits*](#)

Q. 1.1: List the octal and hexadecimal numbers from 16 to 32. Using A and B for the last two digits von Dr. Dhiman Kakati vor 1 Jahr 9 Minuten, 41

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Q. 3.18: Draw a logic diagram using only two-input NOR gates to implement the following function:

*Q. 3.18: Draw a logic diagram using only two-input NOR gates to implement the following function:
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diagram using only two-input NOR gates to implement the following function: $F1A, B, C, D2 = (A \text{ XOR } B)'(C \dots$

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